MC33937 Initialization Requirements

Introduction

The MC33937 and MC33937A provide safe, dependable, gate control for 3 phase Brushless DC (BLDC) motor control units when it is properly configured. However, if improperly initialized, the high side gate drive can be left in a high impedance mode which will allow charge to accumulate from external sources, eventually turning on the high side output transistor. It is prudent to follow a well defined initialization procedure which will establish known states on the gates of all the phase drivers before any current flows in the motor.

Recovery from Sleep Mode (RESET)

The output gate drive is pulled low with the hold-off circuit as long as VLS is low, there is a Power On Reset condition or +5V is low. These conditions are present during a Reset condition. When first coming out of a reset condition, the gate drive circuits are in a high impedance state until the first command is given for operation. After the Reset line goes high, the supplies begin to operate and the hold off circuit is deactivated. The phase input lines will not have any effect on the gate drive until both ENABLE1 and ENABLE2 go high and even then, the low side gate must be commanded on before the high side gate can be operated. This is to insure the bootstrap capacitor has been charged before commencing normal operation. Then the high side gate must be commanded on and then off to initalize the output latches. A proper initialization sequence will place the output gate drives in a low impedance known condition prior to releasing the device for normal operation.

A valid initialization sequence would go something like this:

1. RESET goes high (ENABLE1 and ENABLE2 remain low)
2. SPI commands to configure valid interrupts, DESAT mode and Dead Time are issued
3. SPI command to clear all interrupt conditions
4. ENABLE1 and ENABLE2 are set HIGH (LS outputs are now enabled)
5. PA_LS, PB_LS and PC_LS are toggled HIGH for about 1us (HS outputs are enabled, but not latched)
6. Toggle nPA_HS, nPB_HS and nPC_HS LOW for DEAD TIME plus at least 0.1us (HS outputs are now latched and operational).

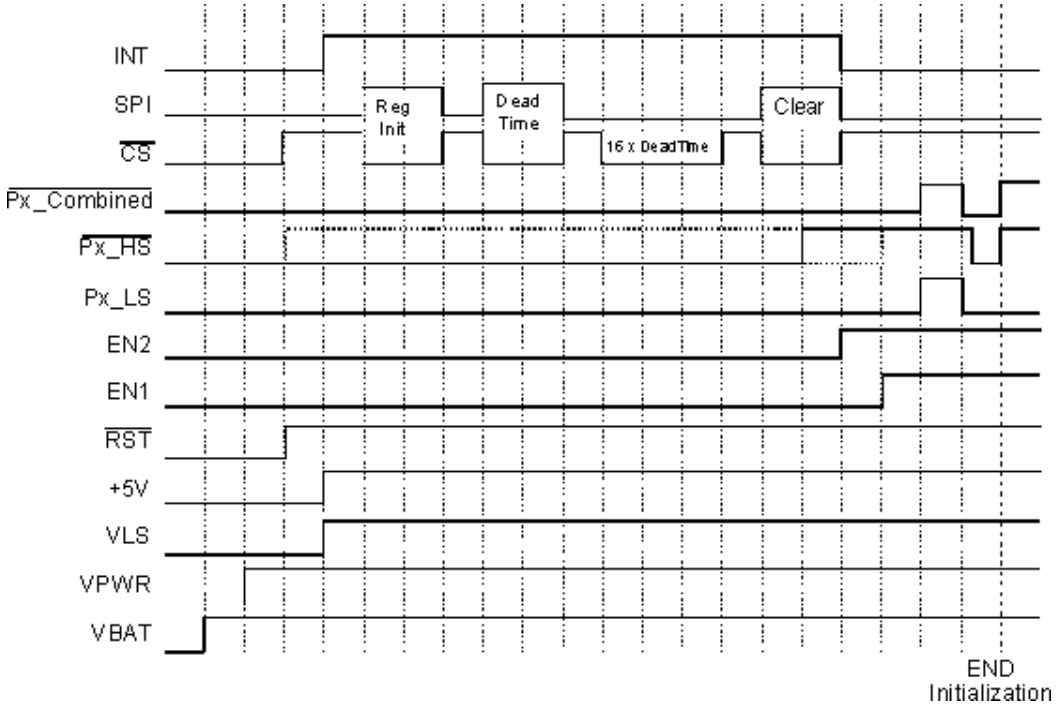
End of initialization.

Doing step 6 simultaneously on all HS inputs will place the motor into HIGH Side Recirculation mode and will not cause motion during the 1us they are ON.

This action will force the High Side gate drive out of tri-state mode and leave it with the HS_G shorted to HS_S on all phases. The HS output FETs will be OFF and ready for normal motor control.

Step 5 and step 6 can be done on all the stated inputs simultaneously. In fact it is desirable for the HS (step 6) to be toggled simultaneously to prevent current from flowing in the motor during initialization.

Note from the specification for the MC33937, the inputs PA_LS, PB_LS, PC_LS, nPA_HS, nPB_HS and nPC_HS are edge sensitive. Toggling the LS inputs enables the HS drivers, so for the HS drivers to be initialized correctly the edge of the input signal to the HS drivers must come after the LS input toggle. A failure to do this will result in the HS gate output remaining in a high impedance mode. This can result in an accumulation of charge, from internal and external leakage sources, on the gate of the HS output FET causing it to turn ON even though the input level to the MC33937 would appear to indicate it should be OFF. When this happens, the logic of the MC33937 will allow the LS output FET to be turned ON without taking any action on the HS gate because the logic is still indicating that the HS gate is OFF. The inital LS input transition from low to high needs to be after both ENABLE inputs are high (the device in NORMAL mode) for the same reason. The delay between ENABLE and the LS input should be 280ns minimum to insure the device is out of STBY mode.



The horizontal divisions are not to scale, they are a reference to show the sequence of operation. Either individual nPx_HS and Px_LS or nPx_Combined may be used. nPx_Combined is defined as both nPx_HS and Px_LS tied together or operated to the same logic level simultaneously.

Once initialized the output gate drives will continue to operate in a low impedance mode as commanded by the inputs until the next reset event.

Recovery from Standby Mode or a Fault

When in Standby Mode or a fault condition causes a shutdown, the Gate outputs are all driven low. The High Side gate drive is then disabled and locked to prevent unauthorized transitions. This requires an initialization sequence to recover normal operation at the end of this mode of operation. The initialization sequence is nearly identical to recovery from Sleep mode, with the modification that the initial pulse to the Low Side Control inputs can be reduced to a 100ns pulse (the Low Side Gates may not actually change state). Then the initialization is completed by cycling the High Side Gates to re-engage the gate drive and insure that that it is in the proper state prior to resuming normal operation.

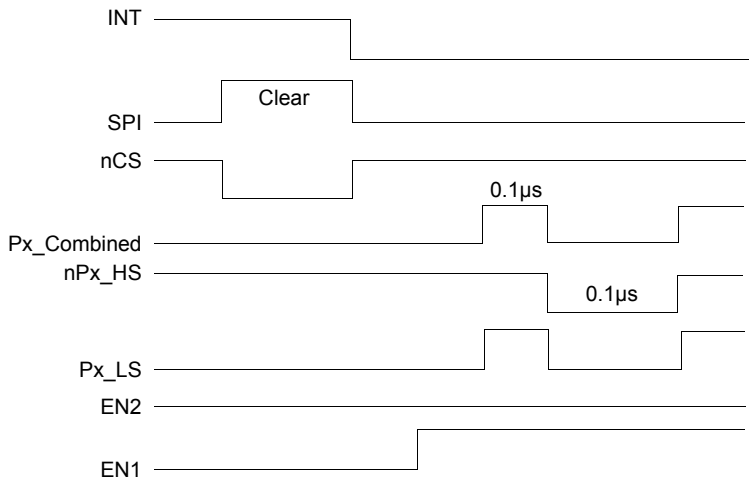
A valid initialization sequence would go something like this:

1. SPI command to clear all interrupt conditions
2. ENABLE1 and ENABLE2 are set HIGH (LS outputs are now enabled)
3. PA_LS, PB_LS and PC_LS are toggled HIGH for at least 100ns (HS Gate Drive outputs are enabled) longer if bootstrap capacitors need charged.
4. Toggle nPA_HS, nPB_HS and nPC_HS LOW for DEAD TIME plus at least 100ns.

End of initialization.

Doing step 4 simultaneously on all HS inputs will place the motor into HIGH Side Recirculation mode and will not cause motion during the 1µs they are ON. This action will restore the High Side gate drive operation and leave it with the HS_G shorted to HS_S on all phases. The HS output FETs will be OFF and ready for normal motor control.

Step 3 and step 4 can be done on all the stated inputs simultaneously. In fact, it is desirable for the HS (step 4) to be toggled simultaneously to prevent current from flowing in the motor during initialization.



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