Freescale Semiconductor
Application Note

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i.MX 6SoloLite Power Consumption Measurement

by *Freescale Semiconductor, Inc.*

This application note helps the user design power management systems. Through several use cases, this report illustrates current drain measurements of the i.MX 6SoloLite system-on-chip (SoC), taken on the Freescale EVK board. The reader will be enabled to choose the appropriate power supply domains for the i.MX 6SoloLite SoC and become familiar with the expected SoC power in different scenarios.

NOTE

Since the data presented in this application note is based on empirical measurements on a small sample size, the results presented are not guaranteed.

Contents

1 Overview of i.MX 6SoloLite Voltage Supplies

The i.MX 6SoloLite SoC has several power supply domains (voltage supply rails) and several internal power domains. Figure 1 shows the connectivity of these supply rails and the distribution of the internal power domains.

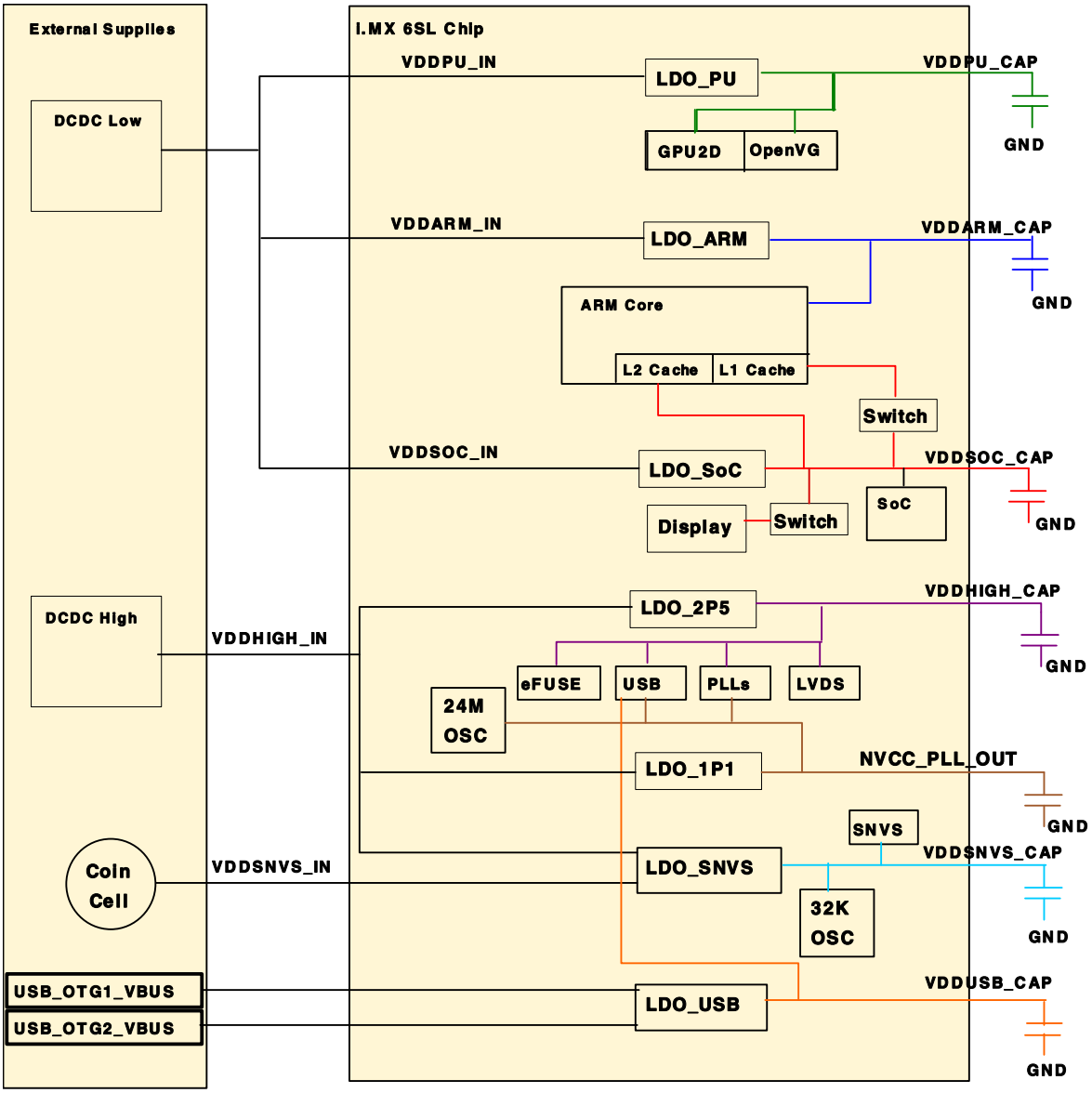

Figure 1. i.MX 6SoloLite Power System

NOTE

See the i.MX 6SoloLite datasheet, for the recommended operating conditions of each supply rail and for a detailed description of the groups of I/Os (pins) each I/O voltage supply powers.

For more details regarding the i.MX 6SoloLite power rails, see Power Management Unit (PMU) chapter in the *i.MX 6SoloLite Multimedia Applications Processors Reference Manual (IMX6SLRM)*.

2 Internal Power Measurement of the i.MX 6SoloLite Processor

Several use cases (described in Section 3, "Use Cases and Measurement Results") are run on the EVK board. The measurements are taken mainly for the following power supply domains—VDDARM_IN, which is the ARM platform's supply, VDDSOC_IN, which is the peripheral supply, VDDHIGH_IN, which is the source of PLLs, DDR pre-drives, PHYs, and some other circuitries, and VDDPU_IN, which is the GPU2D and OpenVG's supply. These supply domains consume the majority of the internal power of the processor. For the relevant use cases, the power of additional supply domains are added. However, the power of these supply domains does not depend on specific use cases, but whether these modules are used or not. The power consumption of SNVS is comparatively negligible except in Deep Sleep Mode.

The NVCC_* power consumption depends primarily on the board level configuration and the components. Therefore, it is not included in the i.MX 6SoloLite internal power analysis. The power of NVCC_DRAM is added for reference.

The power consumption for these supplies, in different use cases, is provided in Table 1 through Table 3.

NOTE

Unless stated otherwise, all the measurements are done on typical process silicon, at room temperature (26 °C approximately).

2.1 Hardware and Software Used

The software versions used for the measurement are as follows:

- Linux version used: Gnome (Linux BSP version 1210 GA) based on Linux kernel version 3.0.35.
- Android version used: Android R13.5.0 GA based on:
  - Google Ice Cream Sandwich 4.0.4 r1.1 release
  - Linux kernel version 3.0.35
- The board used for the measurements is the Freescale i.MX 6SoloLite EVK board.
- The measurements were performed using Agilent 34401A 6 ½ Digit Multimeter.

2.2 Board Setup used for Power Measurements

The power measurements are taken using the following input voltages of the supplies.

- VDDARM_IN and VDDSOC_IN at 1.425 V

- VDDHIGH_IN at 2.78 V
- DRAM_PWR at 1.2 V

Also, the on-chip LDOs are used which is the recommended settings for simplified and cost effective system. The ARM voltage scaling is done through configuring LDO_ARM.

Thus, by using a different setup, such as configurable and separated DC switcher for ARM, the system power may be further optimized by reducing VDDARM_IN input voltage level and match it to the desired operating point. Such setup would likely result in a higher system cost, so there is a trade off between cost versus system power.

The default configuration for LDO is digital bypass for the Linux BSP. ARM voltage is varied by changing the voltage at PMIC level.

2.3 Measuring Points on the Freescale EVK Board

The power data is obtained by measuring the average voltage drop over the measurement points, and dividing it by the resistor value to get the average current. The tolerance of the 0.02 Ω resistors on the SD board is 1%. The measuring points for the various supply domains are as follows:

- VDDSOC—The SOC domain current is measured on SH3 and the recommended resistance value for this measurement is 0.02 Ω.
- VDDCORE—The ARM domain current is measured on SH2 and the recommended resistance value for this measurement is 0.02 Ω.
- VDDHIGH—The VDDHIGH domain current is measured on SH4 and the recommended resistance value for this measurement is 0.1 Ω.
- DDR3 I/O plus Memories—The current in this domain includes the NVCC_DRAM current and the overall current of the on-board LPDDR2 memory devices. The current in this domain is measured on SH25 and the recommended resistance value for this measurement is 0.02 Ω.

3 Use Cases and Measurement Results

3.1 Use Cases

The main use cases and subtypes, which form the benchmarks for i.MX 6SoloLite internal power measurements, are as follows:

- Low power mode
  - Deep Sleep mode
  - System Idle mode
- Audio playback
  - MP3 Audio Playback

NOTE

All measurements in this Application Note are taken at room temperature of 26 °C unless otherwise noted.

3.2 Low Power Mode Use Cases

3.2.1 Use Case 1— Deep Sleep Mode (DSM)

This mode is named as Dormant mode or Suspend to RAM, in the Linux BSP. This is the lowest possible power state where external supplies are still on.

Measurement condition:

- ARM platform is power gated.
- L1 Cache periphery is power gated.
- PU regulator is disabled (means that GPUs and VPU are power gated).
- SoC regulator is not explicitly changed in DSM mode.
- All PLLs (phase locked loop) and CCM (clock controller module) generated clocks are off.
- CKIL (32 KHz) input is on.
- All the modules are disabled.
- Well bias is applied.
- All analog PHYs are powered down.
- External high frequency crystal and on chip oscillator are powered down (by asserting SBYOS bit in CCM).
- VDDARM_IN and VDDSOC_IN are dropped to 0.9 V by asserting the PMIC_STBY_REQ.

In this mode, no current flow is caused by external resistive loads.

Table 1 shows the measurement results when this use case is applied on the i.MX 6SoloLite processor.

Table 1. DSM Measurement Results

Supply Domain	Voltage (V)	Linux GA1209		Voltage (V)	Android R13.4-GA	
		P (mW)	I (mA)		P (mW)	I (mA)
VDD_ARM_IN	0.925	0.013	0.014	0.926	0.046	0.050
VDD_SOC_IN + VDD_PU_IN	0.920	0.506	0.550	0.924	0.601	0.650
VDD_HIGH_IN + NVCC33_IO	3.125	2.028	0.649	3.126	2.032	0.650
VDD_SNVS_IN	3.100	0.050	0.016	3.127	0.156	0.050
Total Power (exclude NVCC_DRAM + LPDDR2)		**2.597**			**2.835**	
NVCC_DRAM + LPDDR2_1V2 (exclude LPDDR2_1V8)	1.190	1.071	0.900	1.194	0.836	0.700
Total Power		3.668			3.671	

NOTE

For additional details on this use case and settings, see Section 5, "Use Cases Configuration and Usage Guidelines."

3.2.2 Use Case 2—System Idle Mode

Measurement condition:

- SoC is in WAIT mode most of the time.
- For lowest power all PLLs are bypassed. If any PLLs are ON, power will be higher.
- Operating system is on.
- EPDC is clock gated.
- Display PMIC is turned OFF.
- Screen is not refreshed.

This use case simulates the situation when the device is left idle for some time and the display is turned off after the timer expires.

Table 2 shows the measurement results when this use case is applied on the i.MX 6SoloLite processor.

Table 2. System Idle Mode Measurement Results

Supply Domain	Voltage (V)	Linux - GA1209	
		P (mW)	I (mA)
VDD_ARM_IN	0.951	2.045	2.150
VDD_SOC_IN + VDD_PU_IN	1.145	3.950	3.450
VDD_HIGH_IN + NVCC33_IO	3.125	8.438	2.700
VDD_SNVS_IN	3.100	0.078	0.025
Total Power (exclude NVCC_DRAM + LPDDR2)		**14.510**	
NVCC_DRAM + LPDDR2_1V2 (exclude LPDDR2_1V8)	1.193	0.895	0.750
Total Power		15.405	

NOTE

For additional details on this use case and settings, see Section 5, "Use Cases Configuration and Usage Guidelines."

3.3 Application Use Cases

3.3.1 MP3 Audio Playback

Measurement condition:

1. MP3 (MPEG-1 audio layer 3) decoding is done by ARM.
2. Audio playback is run through SSI (serial synchronous interface).
3. The stream 128 Kbps_44 kHz_s_mp3.mp3 is taken from the SD (secure digital) card.

Table 3 shows the measurement results when this use case is applied on the i.MX 6SoloLite processor.

Table 3. MP3 Audio Playback Measurement Results

Supply Domain	Voltage (V)	Linux - GA1209	
		P (mW)	I (mA)
VDD_ARM_IN	0.950	17.908	18.850
VDD_SOC_IN + VDD_PU_IN	1.146	32.323	29.950
VDD_HIGH_IN + NVCC33_IO	3.125	79.563	24.500
VDDSNVS_IN	3.100	0.109	0.035
Total Power (exclude NVCC_DRAM + LPDDR2)	**128.901**	**289.88**	
NVCC_DRAM + LPDDR2_1V2 (exclude LPDDR2_1V8)	1.190	10.115	8.500
Total Power		139.016	

NOTE

For additional details on this use case and settings, see Section 5, “Use Cases Configuration and Usage Guidelines.”

4 Reducing Power Consumption

The overall system power consumption depends on both software optimization and how the system hardware is implemented. Below is a list of suggestions which may help to reduce system power. Part of this is already implemented in Linux BSP. Further optimizations can be done on individual customer's system.

NOTE

Further power optimizations are planned to be implemented in future BSP releases. See Freescale website to obtain the latest BSP release.

- Apply clock gating whenever clocks or modules are not used, by configuring CCGR registers in the CCM (Clock Controller Module).
- Reduce the number of operating PLLs—Applicable mainly in Audio Playback mode or Idle modes.
- Core DVFS and system bus scaling—Applying DVFS for ARM and scaling the frequencies of the AXI, AHB, and IPG bus clocks can significantly reduce the power consumption of VDDARM domain and VDDSOC domain, respectively. However, due to the reduced operation frequency, the accesses to the DDR take longer, which increases the power consumption of the DDR I/O and memories. This trade off needs to be taken into account for each mode, to quantify the overall affect on system power.
- Put i.MX 6SoloLite into low power modes (WAIT, STOP) whenever possible. See the CCM chapter of i.MX 6SoloLite reference manual for details.
- DDR interface optimization:
  - Use careful board routing of the DDR memories, maintaining PCB trace lengths as short as possible.
  - Use proper output driver impedance for DDR interface pins which provides good impedance matching. Select the lowest possible drive strength, which still provides the required performance, in order to save current through DDR I/O pins.
  - Carefully choose on-board resistors so the least amount of current is wasted, for example, when selecting impedance matching resistors between CLK and CLK_B (when using DDR3 memories).
  - Float i.MX 6SoloLite DDR interface pins (set to high Z) when DDR memory is in self refresh mode, keeping DDR_SDCKE0 and DDR_SDCKE1 at low value, if done using external pull-down, need to make sure there is no on board termination on these pins during this mode.
  - Use of DDR memory offerings in the latest process technology can significantly reduce the power consumption of the DDR devices and the DDR I/O.

5 Use Cases Configuration and Usage Guidelines

5.1 Deep Sleep Mode (LPM6)

5.1.1 Clocks and PLLs Configuration

In this use case all clocks and PLLs are turned off except 32 KHz clock which is for system wake up.

5.1.2 Steps

Disable ELCDIF and PxP V4L2

```
./ltib -c
```

Choose the following options within LTIB tool to configure the toolchain:

Configure the kernel

Device Drivers --->

Graphics support --->

Support MXC ELCDIF framebuffer <Disable>

Multimedia support --->

Video capture adapters --->

MXC PxP V4L2 driver <Disable>

Run the following command:

```
echo mem > /sys/power/state
```

Use case is running, measurements can be taken now.

5.2 System Idle Mode (LPM2)

5.2.1 Clocks Configuration

Clocks configuration in Table 4 is aligned with release 1210 GA.

Table 4. Clocks Configuration

Clock Name	Frequency (MHz)
AXI	3
AHB	3
CPU	3
GPU2D	off

Table 4. Clocks Configuration (continued)

Clock Name	Frequency (MHz)
GPU3D Core	off
GPU3D Shader	off
VPU	off
IPU1	off
IPU2	off
MMDC CH0	off
MMDC CH1	1

5.2.2 PLLs Configuration

PLLs configuration in Table 5 is aligned with release 1210 GA.

Table 5. PLLs Configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	24
PLL2—System Bus PLL	24
pll2 396m pfd	24
pll2 352m pfd	off
pll2 594m pfd	off
PLL3—OTG USB PLL	off
pll3 508m pfd	off
pll3 454m pfd	off
pll3 720m pfd	off
pll3 540m pfd	off
PLL4—Audio PLL	off
PLL5—Video PLL	off
PLL6—MLB PLL	off
PLL7—Host USB PLL	off
PLL8—ENET PLL	off

5.2.3 System Setup

Disconnect everything except the SD and LVDS.

5.2.4 Steps

1. Boot kernel with command debug_uart2.
2. Run below script:

```
#!/bin/sh -x
echo 1 > /sys/class/graphics/fb0/blank
ifconfig eth0 down
mount -t debugfs nodev /sys/kernel/debug
axi=$(find /sys/kernel/debug -name axi_clk)

sleep 25
```

```
axi_rate=$(cat $axi/rate)

while [ $axi_rate -ne 24000000 ]; do
sleep 1
echo "need wait more"
axi_rate=$(cat $axi/rate)
done
```

5.3 Audio Playback

5.3.1 Clocks Configuration

Clocks configuration in Table 6 is aligned with release 1210 GA.

Table 6. Clocks Configuration

Clock Name	Frequency (MHz)
AXI	50
AHB	24
CPU	400 when active, 24 when in WFI
GPU2D	off
GPU3D Core	off
GPU3D Shader	off
VPU	off
IPU1	off
IPU2	off
MMDC CH0	off
MMDC CH1	50

5.3.2 PLLs Configuration

PLLs configuration in Table 7 is aligned with release 1210 GA.

Table 7. PLLs Configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	off
PLL2—System Bus PLL	528
pll2 396m pfd	on
pll2 352m pfd	off

Table 7. PLLs Configuration (continued)

PLL Name	Frequency (MHz)
pll2 594m pfd	off
PLL3—OTG USB PLL	off
pll3 508m pfd	off
pll3 454m pfd	off
pll3 720m pfd	off
pll3 540m pfd	off
PLL4—Audio PLL	176
PLL5—Video PLL	off
PLL6—MLB PLL	off
PLL7—Host USB PLL	off
PLL8—ENET PLL	off

5.3.3 System Setup

- SD boot
- Connect XGA LVDS panel

5.3.4 Steps

1. Add enable_wait_mode=on in kernel command line.
2. Boot system to SD rootfs with LVDS, run the below commands to enable busfreq scaling:

```
#!/bin/sh
echo 1 > /sys/class/graphics/fb0/blank
echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
ifconfig eth0 down
```

If it does not run into low busfreq automatically, run the following commands:

```
echo 1 > /sys/devices/platform/imx_busfreq.0/enable
```

3. Run the following command:

```
gplay 128kbps_44khz_s_mp3.mp3
```

4. Measure SoC and Arm data, and record.

5.4 Important Commands

In Boot Console,

- `printenv`—Display environment variables.
- `setenv`—Update environment variables.

  `setenv <name> <value> ...–Set environment variable ‘name’ to ‘value ...’`

  `setenv <name>–Delete environment variable ‘name.’`
- `saveenv`—Save updates to environment variables.
- `bootargs`—Pass to the kernel, which are called kernel command lines.

In Linux Console,

- `cat /proc/cmdline`—Displays command line
- `cat /sys/devices/virtual/thermal/thermal_zone0/temp`—Print temperature to screen (chip should be calibrated)
- In order to print to screen clocks configuration, use the `clocks.sh` script.

clocks.sh:

```
#!/bin/bash

saved_path=$PWD

if ! mount|grep -sq '/sys/kernel/debug'; then
    mount -t debugfs none /sys/kernel/debug
fi

printf "%-24s %-20s %3s %9s\n" "clock" "parent" "use" "flags" "rate"

for foo in $(find /sys/kernel/debug/clock -type d); do
    if [ "$foo" = '/sys/kernel/debug/clock' ]; then
        continue
    fi

    cd $foo

    ec="$(cat usecount)"
    rate="$(cat rate)"
    flag="$(cat flags)"
```

```
        clk="$(basename $foo)"
        cd ..
        parent="$(basename $PWD)"

        if [ "$parent" = 'clock' ]; then
        parent="   ---"
        fi

        printf "%-24s %-24s %2d %2d %10d\n" "$clk" "$parent" "$ec" "$flag" "$rate"
        cd $saved_path
    done
```

6 Revision History

Table 8 provides a revision history for this application note.

Table 8. Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 0	12/2012	Initial public release.

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